The Applicant appreciates the Examiner's thorough examination of the subject application and respectfully requests reconsideration of the subject application based on the above amendments and the following remarks.

35 U.S.C. § 103(a) REJECTIONS

The Examiner has rejected claims 1-5 and 7 under 35 USC 103(a) as being unpatentable over the prior art in view of British Patent Application No. (GB 2,307,344A) (the "British Application") and, further, has rejected claims 6 and 8 as being unpatentable over the prior art in view of U.S. Patent Number 4,986,878 to Malazgirt, et al. ("Malazgirt" or the "Malazgirt Reference"). The Applicant respectfully traverses these rejections for reasons detailed below.

According to the Examiner, the admitted prior art discloses all of the features of the invention as claimed except for a planar/flat top surface, which the Examiner maintains is taught by the British Application. The Applicant respectfully disagrees.

The British Application is directed to a method of forming a planarized passivation layer of a semiconductor device, i.e., a field effect transistor (FET), which is not a solid-state imaging device. The purpose of this method is to flatten the passivation layer to improve the insulation of the device. More specifically, the British Application teaches a method for planarizing a semiconductor device by diffusing dopants from a planarization layer 18 in a first annealing step, which is followed by a second annealing step after which a thermal oxide layer 19 is formed thereon. See, e.g., British Application, Abstract; FIG. 2E. In so doing, the surface of a silicon wafer can be planarized "without the precipitation of dopants taking place." Id., page 7, lines 18-19. Thus, there is nothing in the British Application that teaches, mentions, suggests or provides a motive to provide a non-stepped passivation layer 5 to improve light incidence.

Indeed, planarization, or flattening, of the passivation film 5 of the present invention is for the purpose of converging incident light onto a light reception section 2. Prior art solid-state imaging devices included stepped passivation films 15, which made it difficult to converge incident light on the light reception section 12 because stepped surfaces associated with the prior art reflected and refracted light. See, e.g., Application page 8, line 7 to page 9, line 9. Thus, there is nothing in the prior art that teaches, mentions, suggests or provides a motivation to planarize the stepped passivation layers 5 of solid state imaging devices to enhance light convergence.

Accordingly, the admitted prior art does not teach, mention or suggest the invention as claimed. Furthermore, the British Application cannot make up for the deficiencies of the admitted prior art. Thus, it is respectfully submitted that, claims 1-5 and 7 are not made obvious by the admitted prior art in view of the British Application and, further, satisfy the requirements of 35 U.S.C. 100, et seq., especially § 103(a). Accordingly, claims 1-5 and 7 are allowable. Moreover, it is respectfully submitted that the subject application is in condition for allowance. Early and favorable action is requested.

With respect to claims 6 and 8, according to the Examiner, the admitted prior art discloses all of the features of the invention as claimed except for forming the passivation section to have a substantially flat top surface. Moreover, the Examiner maintains that, the Malazgirt reference teaches flattening the top surface by chemical machine polishing or forming an insulation section. The Applicant respectfully disagrees.

The Malazgirt reference teaches a process for planarizing the surface of a semiconductor device to overcome two shortcomings in the prior art: cracking of an SOG film in the space between metal interconnects and inadequate adhesion of SOG film to bare metal lines. See, e.g., Malazgirt, col. 3, lines 28-34. Specifically, the Malazgirt process includes the steps of depositing a dielectric layer over the semiconductor device(s); applying a layer of spin-on-glass (SOG) to the surface of the

dielectric layer; etching away portions of the SOG and dielectric layers; and then removing all remaining portions of the SOG before applying a passivation layer. See, e.g., col.6, line 35 to col. 9, line 59; Claim 1. Thus, Malazgirt teaches applying an SOG before applying a passivation layer and removing the SOG layer completely by etching. Accordingly, Malazgirt does not teach, mention or suggest the present invention in which a P-SiN passivation film is deposited on the light-shielding film 4 and then SOG is applied to the P-SiN passivation film. The top of the passivation film is then flattened by etching and a planarization film 6 is applied to the substantially flattened passivation layer. Claim 6 distinctly claims:

> forming a thin film used for forming the passivation section on the light shielding section; [and]
> applying an SOG film to the thin film used for forming the passivation section.

Thus, with the invention as claimed, the SOG is applied after application of the passivation layer and the SOG remains in the final formed device. Indeed, Malazgirt teaches away from leaving any SOG on the integrated circuit. Moreover, Malazgirt does not teach, mention or suggest a method of producing a solid-state imaging device that enables one to converge incident light onto a light receiving section thereof.

Accordingly, Malazgirt reference cannot make up for the deficiencies of the admitted prior art. Thus, it is respectfully submitted that, claims 6 and 8 are not made obvious by the admitted prior art in view of the Malazgirt reference and, further, satisfy the requirements of 35 U.S.C. 100, et seq., especially § 103(a). Accordingly, claims 6 and 8 are allowable. Moreover, it is respectfully submitted that the subject application is in condition for allowance. Early and favorable action is requested.

The Applicant believes that no additional fee is required for consideration of the within Response. However, if for any reason the fee paid is inadequate or credit is owed for any excess fee paid, you are hereby authorized and requested to charge Deposit Account No. **04-1105**.

Respectfully submitted,

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By: _____
George W. Hartnell, III
Reg. No. 42,639
Attorney for Applicant(s)

Dike, Bronstein, Roberts & Cushman
Intellectual Property Practice Group
EDWARDS & ANGELL, LLP
P.O. Box 9169
Boston, MA 02209
(617) 517-5523
Customer No. 21874
316922

ANNEX TO AMENDMENT

MARKED UP VERSIONS OF AMENDED CLAIMS

IN THE CLAIMS

6. (Amended) A method for producing a solid-state imaging device, wherein the device comprises:

a semiconductor substrate;

a light shielding section having an aperture for partially shielding light incident on a surface of the semiconductor substrate;

a light reception section for converting the light which is incident on the surface of the semiconductor substrate through the aperture to an electric charge; and

a passivation section having a substantially flat top surface and overlying the light shielding section, the light reception section and the aperture so as to provide moisture and chemical resistance and to provide barrier properties against impurities, wherein the method comprises the steps of:

forming a thin film used for forming the passivation section on the light shielding section;

applying an SOG film to the thin film used for forming the passivation section; and

flattening a surface of the thin film to form the passivation section by performing an etchback technique under a condition that a selective ratio of the SOG film to the thin film used for forming the passivation section is about 1:1.

7. (Amended) A method for producing a solid-state imaging device, wherein the device comprises:

a semiconductor substrate;

a light shielding section having an aperture for partially shielding light incident on a surface of the semiconductor substrate;

a light reception section for converting the light which is incident on the surface of the semiconductor substrate through the aperture to an electric charge; and

a passivation section having a substantially flat top surface and overlying the light shielding section, the light reception section and the aperture so as to provide moisture and chemical resistance and to provide barrier properties against impurities, and an insulation section having a substantially flat top surface which is interposed between the passivation section and the light shielding section, wherein the method comprises the steps of:

forming the insulation section on the light shielding section;

flattening a surface of the insulation section by chemical machine polishing; and

forming the passivation section so as to have the substantially flat top surface by depositing a material used for forming the passivation section on the insulation section.

8. (Amended) A method for producing a solid-state imaging device, wherein the device comprises:

a semiconductor substrate;

a light shielding section having an aperture for partially shielding light incident on a surface of the semiconductor substrate;

a light reception section for converting the light which is incident on the surface of the semiconductor substrate through the aperture to an electric charge;

a passivation section having a substantially flat top surface and overlying the light shielding section, a light reception section and the aperture;

an insulation section having a substantially flat top surface which is interposed between the passivation section and the light shielding section so as to provide moisture and chemical resistance and to provide barrier properties against impurities, wherein the method comprises the steps of:

forming the insulation section so as to have the substantially flat top surface by applying an SOG film to the light shielding section and the aperture; and

forming the passivation section so as to have the substantially flat top surface by depositing a material used for forming the passivation section on the insulation section.